1. A method of forming a metal oxide semiconductor field effect transistor (MOSFET) device, with a gate insulator layer comprised of a high dielectric constant (high k), dielectric layer, on a semiconductor substrate, comprising the steps of:

forming a well region in a top portion of said semiconductor substrate;

forming a hard mask on a portion of top surface of said semiconductor substrate;

performing a first dry etch procedure to remove a top portion of said semiconductor substrate not covered by said hard mask, resulting in recessed regions in said semiconductor substrate, and a non-recessed portion of said semiconductor substrate covered by said hard mask;

forming a heavily doped source/drain region in a top portion of said recessed regions;

depositing a polysilicon layer;

performing a second dry etch procedure to form lightly doped source/drain (LDD), polysilicon spacers on the sides of said non-recessed portion of said semiconductor substrate;

forming a metal silicide region in a top portion of said heavily doped source/drain region;

forming a planarized first insulator layer, exposing top surface of said hard mask;

removing said hard mask resulting in space located between LDD polysilicon spacers, exposing top surface of underlying said non -recessed portion of said semiconductor substrate;

forming said gate insulator layer, comprised of said high k dielectric layer, in said space; and

forming a conductive metal structure on said gate insulator layer.

2. The method of claim 1, wherein said well region is a P well region, obtained via implantation of boron or BF_2 ions, at an energy between about 150 to 250 KeV, at a dose between about 1E13 to 1E14 atoms/cm^2.

3. The method of claim 1, wherein said well region is an N well region, obtained via implantation of arsenic or phosphorous ions, at an energy between about 300 to 600 KeV, at a dose between about 1E13 to 1E14 atoms/cm^2.

4. The method of claim 1, wherein said hard mask is a silicon nitride shape, formed from a silicon nitride layer, in turn obtained via LPCVD or PECVD procedures, at a thickness between about 10 to 500 Angstroms.

5. The method of claim 1, wherein the depth of said recessed regions in said semiconductor substrate is between about 100 to 100,000 Angstroms.

6. The method of claim 1, wherein said heavily doped source/drain region is a P type, heavily doped source/drain region, obtained via implantation of boron or BF_2 ions, at an energy between about 1 to 50 KeV, and at a dose between about 1E12 to 5E15 atoms/cm^2.

7. The method of claim 1, wherein said heavily doped source/drain region is an N type, heavily doped source/drain region, obtained via implantation of arsenic or phosphorous ions, at an energy between about 10 to 150 KeV, and at a dose between about 1E12 to 1E16 atoms/cm^2.

8. The method of claim 1, wherein said polysilicon layer is a P type in situ doped polysilicon layer, obtained via LPCVD procedures at a thickness between about 100 to 5000 Angstroms, and doped via the addition of diborane to a silane ambient.

9. The method of claim 1, wherein said polysilicon layer is an N type in situ doped polysilicon layer, obtained via LPCVD procedures at a thickness between about 100 to 5000 Angstroms, and doped via the addition of arsine, or phosphine, to a silane ambient.

10. The method of claim 1, wherein second dry etch procedure, used to form said LDD polysilicon spacers, is an anisotropic RIE procedure, using Cl_2 or SF_6 as an etchant for said in situ doped polysilicon layer.

11. The method of claim 1, wherein said hard mask is selectively removed via wet etch procedures using a hot phosphoric acid solution.

12. The method of claim 1, wherein said hard mask is selectively removed via a dry etch procedure using Cl_2 as an etchant.

13. The method of claim 1, wherein said high k dielectric layer, used for said gate insulator layer, is comprised of either aluminum oxide (Al_2O_3), zirconium oxide (ZrO_2), or hafnium oxide (HfO_2), obtained at a thickness between about 10 to 1000 Angstroms, via metal organic chemical vapor deposition (MOCVD), or via atomic layer chemical vapor deposition (ALCVD) procedures, performed at a temperature between about 100 to 1000° C, using $HfCl_4$ or $ZrCl_4$ as reactants for the ALCVD procedure, or using tetrakis dimethyl amino hafnium (TDMAH), or TDMAZ), as reactants for the MOCVD procedure.

14. The method of claim 1, wherein said high k dielectric layer is comprised with a dielectric constant between about 7 to 100.

15. The method of claim 1, wherein said conductive gate structure is comprised of either a metal layer such as tungsten, aluminum, aluminum - copper, or copper, a metal silicide layer such as tungsten silicide, or a doped polysilicon layer.

16. A method of fabricating a complementary metal oxide semiconductor (CMOS) device on a semiconductor substrate, comprised of a P channel metal oxide semiconductor (PMOS), device, and of an N channel metal oxide semiconductor (NMOS), device, and featuring a gate insulator layer comprised of a high k metal oxide layer formed after completion of high temperature process steps, comprising the steps of:

providing a PMOS region in a first area of said semiconductor substrate to be used for said PMOS device, and providing an NMOS region in a second area of said semiconductor substrate to be used for said NMOS device;

forming an N well region in a top portion of said PMOS region;

forming a P well region in a top portion of said N well region;

depositing a silicon nitride layer;

performing a first anisotropic RIE procedure to define a silicon nitride shape, and to recess a top portion of said semiconductor substrate, in said PMOS and in said NMOS regions, resulting in a non-recessed portion of said semiconductor substrate, overlaid by said silicon nitride shape, in said PMOS region and in said NMOS regions;

performing a first ion implantation procedure to form a P type heavily doped source/drain region in a first recessed region located in said PMOS region;

performing a second ion implantation procedure to form an N type heavily doped source/drain region in a second recessed region located in said NMOS region;

depositing a first silicon oxide layer;

removing portion of said first silicon oxide layer located in said PMOS region;

depositing a P type, in situ doped polysilicon layer;

depositing a second silicon oxide layer;

removing portion of said second silicon oxide layer, portion of said P type, in situ doped polysilicon layer, and portion of said first silicon oxide layer located in said NMOS region;

depositing an N type, in situ doped polysilicon layer;

removing portion of said N type, in situ doped polysilicon layer and portion of said second silicon oxide layer located in said PMOS region, resulting in a remaining portion of said P type, in situ doped polysilicon layer in said PMOS region, and resulting in a remaining portion of said N type, in situ doped polysilicon layer located in said NMOS region;

performing a second anisotropic RIE procedure to form P type polysilicon, lightly doped source/drain (LDD), spacers on the sides of non-recessed portion of said semiconductor substrate and on the sides of a bottom portion of said silicon nitride shape, in said PMOS region, and to form N type polysilicon, LDD spacers on the sides of non-recessed portion of said semiconductor substrate and on the sides of a bottom portion of said silicon nitride shape, in said NMOS region;

depositing a first metal layer;

performing a patterning procedure to define metal shapes on the top surface of said P type heavily doped source/drain region, and on the top surface of said N type heavily doped source/drain region;

performing an anneal procedure to form metal silicide regions in said P type heavily doped source/drain region, and in said N type heavily doped source/drain region;

depositing a first insulator layer;

performing a chemical mechanical polishing procedure planarizing top surface of said first insulator layer and exposing the top surface of the silicon nitride shapes;

removing said silicon nitride shapes resulting in spaces located between polysilicon LDD spacers, exposing the top surfaces of the recessed portions of said semiconductor substrate;

depositing said high k metal oxide layer, completely filling said spaces;

depositing a second metal layer;

performing a third anisotropic RIE procedure to define metal gate structures, and to define gate insulator shape, comprised of said high k metal oxide layer;

depositing a second insulator layer;

forming contact hole openings in a second insulator layer and in said first insulator layer, exposing portions of top surfaces of said P type heavily doped source/drain region, of said N type heavily doped source/drain region, and of said metal gate structures; and

forming metal contact structures in said contact hole openings.

17. The method of claim 16, wherein said silicon nitride layer is obtained via LPCVD or PECVD procedures, at a thickness between about 10 to 500 Angstroms.

18. The method of claim 16, wherein the depth of said recess, located in said top portion of said semiconductor substrate, is between about 100 to 100,000 Angstroms.

19. The method of claim 16, wherein said first ion implantation procedure used to create said P type heavily doped source/drain region, is performed via implantation of boron or BF_2 ions, at an energy between about 1 to 50 KeV, and at a dose between about 1E12 to 5E15 atoms/cm^2.

20. The method of claim 16, wherein said second ion implantation procedure used to create said N type heavily doped source/drain region, is performed via implantation of arsenic or phosphorous ions, at an energy between about 10 to 150 KeV, and at a dose between about 1E12 to 1E16 atoms/cm^2.

21. The method of claim 16, wherein said P type, in situ doped polysilicon layer is obtained via LPCVD procedures at a thickness between about 100 to 5000 Angstroms, and doped via the addition of diborane to a silane ambient.

22. The method of claim 16, wherein said N type, in situ doped polysilicon layer is obtained via LPCVD procedures at a thickness between about 100 to 5000 Angstroms, and doped via the addition arsine, or phosphine, to a silane ambient.

23. The method of claim 16, wherein second anisotropic RIE procedure, used to form said P type polysilicon, LDD spacers and said N type polysilicon, LDD spacers, is performed using Cl_2 or SF_6 as an etchant for polysilicon.

24. The method of claim 16, wherein said silicon nitride shapes are selectively removed via wet etch procedures using a hot phosphoric acid solution.

25. The method of claim 16, wherein said silicon nitride shapes are selectively removed via a dry etch procedure using Cl_2 as an etchant.

26. The method of claim 16, wherein said high k metal oxide layer used for said gate insulator layer is comprised of either aluminum oxide (Al_2O_3), zirconium oxide (ZrO_2), or hafnium oxide (HfO_2), obtained at a thickness between about 10 to 1000 Angstroms, via metal organic chemical vapor deposition (MOCVD), or via atomic layer chemical vapor deposition procedures, performed at a temperature between about 100 to 1000° C, using $HfCl_4$ or $ZrCl_4$ as reactants for the ALCVD procedure, or using tetrakis dimethyl amino hafnium (TDMAH), or TDMAZ), as reactants for the MOCVD procedure.

27. The method of claim 16, wherein said high k metal oxide layer is comprised with a dielectric constant between about 7 to 100.

28. The method of claim 16, wherein said second metal layer, used for said metal gate structures, is either a tungsten, aluminum, aluminum - copper, or copper layer.

29. The method of claim 16, wherein said metal gate structures are defined from a metal silicide layer such as tungsten silicide, or from a doped polysilicon layer.

30. A complimentary metal oxide semiconductor (CMOS), device, featuring a P channel metal oxide semiconductor (PMOS), component in a first region of a semiconductor substrate, and featuring an N channel metal oxide semiconductor (NMOS), component in a second region of said semiconductor substrate, comprising:

a P well region located in a top portion of said first region of said semiconductor substrate, and an N well region located in a top portion of said second region of said semiconductor substrate;

an insulator filled, shallow trench isolation region, located in a top portion of said semiconductor substrate between said P well region and said N well region;

a recessed P well region located in the perimeter of said P well region, with a non-recessed P well portion of said semiconductor substrate located in the center of said P well region, surrounded by said recessed P well region;

a recessed N well region located in the perimeter of said N well region, with a non-recessed N well portion of said semiconductor substrate located in the center of said N well region, surrounded by said recessed N well region;

a heavily doped P type source/drain region, located in a top portion of said recessed P well region;

a heavily doped N type source/drain region, located in a top portion of said recessed N well region;

first metal silicide layers located in top portions of said heavily doped P type source/drain region, and second metal silicide layers located in top portions of said N type heavily doped source/drain region;

a first metal oxide gate insulator layer located overlying the top surface of said non-recessed P well portion of said semiconductor substrate, and a second metal oxide gate insulator layer overlying the top surface of said non-recessed N well portion of said semiconductor substrate;

vertical P type silicon spacers located on the sides of said non- recessed P well portion of said semiconductor substrate, and located on the sides of a bottom portion of a first metal oxide gate insulator layer;

vertical N type silicon spacers located on the sides of said non- recessed N well portion of said semiconductor substrate, and located on the sides of a bottom portion of a second metal oxide gate insulator layer;

conductive gate structures located overlying the metal oxide gate insulator layers;

an interlevel dielectric (ILD) layer located overlying said conductive gate structures;

contact hole openings in said ILD layer exposing top surface of said conductive gate structures, and exposing top surface of said heavily doped P type source/drain region, and of said heavily doped N type source/drain region; and

metal structures located in said contact hole openings.

31. The CMOS device of claim 30, wherein the depth of said recessed P well region, located in perimeter of said P well region, and of said recessed N well region, located in perimeter of said N well region, is between about 100 to 100,000 Angstroms.

32. The CMOS device of claim 30, wherein said vertical P type silicon spacers, and said vertical N type silicon spacers, are comprised of polysilicon.

33. The CMOS device of claim 30, wherein said metal oxide gate insulator layers are comprised of either aluminum oxide (Al_2O_3), zirconium oxide (ZrO_2), or hafnium oxide (HfO_2), at a thickness between about 10 to 1000 Angstroms, and with said metal oxide gate insulator layers comprised with a dielectric constant between about 7 to 100.

34. The CMOS device of claim 30, wherein said conductive gate structures are comprised of either tungsten, aluminum, aluminum - copper, copper, tungsten silicide, or doped polysilicon.

35. A metal oxide semiconductor field effect transistor (MOSFET) device, comprising:

a well region located in a top portion of a semiconductor substrate;

a recessed well region located in the perimeter of said well region, with a non-recessed well portion of said semiconductor substrate located in the center of said well region, surrounded by said recessed well region;

a heavily doped source/drain region located in a top portion of said recessed well region;

metal silicide layers located in top portions of said heavily doped source/drain region;

a metal oxide gate insulator layer located overlying the top surface of said non-recessed well portion of said semiconductor substrate;

vertical silicon spacers located on the sides of said non- recessed well portion of said semiconductor substrate, and located on the sides of a bottom portion of said metal oxide gate insulator layer;

a conductive gate structure located overlying said metal oxide gate insulator layer;

an interlevel dielectric (ILD) layer located overlying said conductive gate structure;

contact hole openings in said ILD layer exposing top surface of said conductive gate structure, and exposing top surface of said heavily doped source/drain region; and

metal structures located in said contact hole openings.

36. The MOSFET device of claim 35, wherein said well region is a P type well region.

37. The MOSFET device of claim 35, wherein said well region is an N type well region.

38. The MOSFET device of claim 35, wherein the depth of said recessed well region, located in perimeter of said well region, is between about 100 to 100,000 Angstroms.

39. The MOSFET device of claim 35, wherein said vertical silicon spacers are comprised of either P type doped polysilicon or of N type doped polysilicon.

40. The MOSFET device of claim 35, wherein said metal oxide gate insulator layer is comprised of either aluminum oxide (Al_2O_3), zirconium oxide (ZrO_2), or hafnium oxide (HfO_2), at a thickness between about 10 to 1000 Angstroms, and with said metal oxide gate insulator layer comprised with a dielectric constant between about 7 to 100.

41. The MOSFET device of claim 35, wherein said conductive gate structure is comprised of either tungsten, aluminum, aluminum - copper, copper, tungsten silicide, or doped polysilicon.